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A Survey Paper on Leakage Power and Delay in CMOS Circuits

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ABSTRACT

Power consumption is one of the top issues of VLSI circuit design, for which CMOS is the primary technology. Today's focus on low power is not only because of the recent growing demands of mobile applications. Even before the mobile era, power consumption has been a fundamental problem. To solve the power dissipation problem, many researchers have proposed different ideas from the device level to the architectural level and above. However, there is no universal way to avoid tradeoffs between power, delay and area and thus, designers are required to choose appropriate techniques that satisfy application and product needs. In this paper we study different author's paper to relate to this problem and try to find out the best solution for future work.

KEYWORDS: *VLSI, power consumption*

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I. INTRODUCTION

As the technology scales downs, below 100nm, reduction of power consumption and overall power management on single chip have become primary design issue. Power optimization is also important for many designs to minimize package cost and maximize battery back-up of system. Today, electronic devices play a very important role in every one's day to day life. Devices such as mobile phone, i_{pad}, laptop, pocket calculator become necessity to live a comfortable life. Consumer prefers portable and battery powered electronic devices. Earlier in 1990's, performance and speed was the important parameters to design any system but now with the growing trend towards portable computing and wireless communication, power dissipation has become one of the most critical factor in the continued development of microelectronics technology [1]. Different techniques have been studied to reduce these dissipations such as Multiple Supply Voltage scheme, Multiple Threshold Voltage method, Adaptive Body Biasing, Transistor Stacking, Power Gating, Gate Sizing, Clock Gating, Voltage and Frequency Scaling etc.

II. LITERATURE SURVEY

This section presents an organized and comprehensive literature survey in the area of power dissipation in digital circuit design. Survey includes the different power optimization methods at various level of digital circuit design process from system level to physical level. Different sources responsible for power dissipation in complementary metal oxide semiconductor circuits are also reviewed. Techniques to reduce the effect of such sources in different research articles are discussed here.

AfshinAbdollahiet. al., describes two runtime methods in their research paper to reduce leakage current in Complementary metal oxide semiconductor circuits. In both methods it is assumed that the device will produce a 'sleep signal' to indicate the circuit is in standby mode. In first method, pre-selected internal signals and a new set of external inputs are shifted by 'sleep' signal into the circuits. All internal signals are set to logic values to achieve minimum total leakage current in the circuit. Since the leakage current in a CMOS gate is mainly dependent on the combinations of logic values applied to input signals. Hence such method reduces leakage current in Complementary metal oxide semiconductor device. In another method, to increase the controllability of internal signal and to decrease the leakage current through the CMOS gates, the pMOS and nMOS transistors are added to few gates in the circuit using stacking mechanism. An experimental result of such methods on combinational circuits reduces 25% of leakage current and 5% of propagation delay. Similarly, on sequential circuits, implementation of such methods reduces the leakage current by an average of 25% with practically no delay penalty.

Kaushik Roy et. Al, reviewed all causes of leakage current in transistor that includes gate drain leakage, gate-oxide tunneling, drain-induced barrier lowering and weak inversion effect. They observed that the low threshold voltages, gate leakage and sub-threshold voltages are the dominant sources of leakage current in deep sub-micron meter devices. Effect of such sources will increase with technology scaling. The GIDL and BTBT (base to base

tunneling) may also have a significant effect on advanced CMOS devices. The solution should be considered both at circuit level and process technology level in deep sub-micron meter CMOS circuits.

A. Agarwal et.al, All internal signals are set to logic values to achieve minimum total leakage current in the circuit. Since the leakage current in a CMOS gate is mainly dependent on the combinations of logic values applied to input signals. Hence such method reduces leakage current in Complementary metal oxide semiconductor device. In another method, to increase the controllability of internal signal and to decrease the leakage current through the CMOS gates, the pMOS and nMOS transistors are added to few gates in the circuit using stacking mechanism. An experimental result of such methods on combinational circuits reduces 25% of leakage current and 5% of propagation delay.

Priti Shrivastava, Dr.Bharti Chourasia in this paper author discussed Approximate computing has received significant attention as a promising strategy to enhance performance of multiplication. Various arithmetic operations such as multiplication addition, subtraction are important part of digital circuit to speed up the computation speed of processor[35]. This paper presents 32 bit approximate multiplier for high speed and low delay for advance digital signal processing. Previous it is designed at 16 bit for various applications. Research work is focus on hardware-level approximation by introducing the partial product perforation technique and dadda multiplier for designing approximate multiplication circuits. Xilinx 14.7 is used to implementation with verilog programming language.[35]

Warren Shum and Jason H. Anderson, presented an analysis of glitch power in FPGAs and a method for glitch reduction using don't-cares in logic synthesis. A novel glitch reduction technique was presented that sets don't-cares in FPGA configuration bits in order to avoid glitch transitions. This method is performed after placement and routing, and has no effect on circuit area or performance.

Jing Yang and Yong-Bin Kim, describes two runtime methods in their research paper to reduce leakage current in CMOS circuits. In both methods it is assumed that the device will produce a 'sleep signal' to indicate the circuit is in standby mode. In first method, pre-selected internal signals and a new set of external inputs are shifted by 'sleep' signal into the circuits. All internal signals are set to logic values to achieve minimum total leakage current in the circuit. Since the leakage current in a CMOS gate is mainly dependent on the combinations of logic values applied to input signals.

Sheetal Sahani and Dr. Bharti Chourasia, This paper presents a design methodology using CMOS transistor for the architecture of full adder design with minimum number of transistor i.e. reduced size and reduced area for low power consumption in CMOS 90nm technology [29]. This is used to implement low power full adder design for carrying out summation of three different input bits. The circuit of low power full adder is designed by using DSCH tool 2.7 & analysis of the low power full adder design is done at room temperature in CMOS 90 nm technology by using Micro wind tool 2.6.The result shows the comparison in CMOS technology at 90 nm rule on the design in regards of power dissipation, signal propagation delay, transistor counts and power delay product. A comparison is also carried out by some of the parameters taking into consideration like delay of the low power full adder circuit design with the base paper full adder design, which shows the advantage of the proposed low power full adder design. We are using two different simulation tools such as DSCH 2.7 for circuit design and Micro-wind 2.6 for waveform simulation. Firstly the low power full adder circuit will be designed using DSCH tool 2.7 using 10 transistor maintaining W/L ratio 3:1. Then the Verilog code of the design is made and the layout will be made in CMOS 90 nm technology using micro-wind tool 2.6. The low power full adder circuit using 10T design will be simulated at room temperature in CMOS 90 nm technology to compare different parameters like power consumption, delay, PDP & transistor counts.[29]

Zia Abbas and MauroOlivieri this paper presented a detailed study of leakage current mechanisms in CMOS image sensors. They investigated reverse current–voltage characteristics of sensors at 0.045 μm CMOS technology. They conclude that in p-n junction of MOS transistor, tunneling and ionization impact are the dominant mechanisms for leakage current. Similarly thermal Shockley–Read–Hall generation is the main leakage source for n-well/p-well of transistor.

Md Dilnawaz Hansala and Dr. Neetesh Raghuwanshi, discussed Multipliers play a vital job in the present digital signal handling and different applications[34]. With advances in innovation, numerous scientists have attempted and are endeavoring to structure multipliers which offer both of the following plan targets – high speed, low power utilization, consistency of design and henceforth less zone or even mix of them in one multiplier in this way making them appropriate for different high speed, low power and minimal VLSI usage.[34]

III. Problem Formulation

For designing any digital circuits, the main performance parameters are power, delay and area. Circuit which consume low power, less delay and occupies less area is considered as best circuit. Portability imposes a strict limitation on power dissipation with the demands of high computational speeds. Therefore, in present VLSI digital systems the power-delay product becomes the most important metric of performance [3]. The definitions of these parameters are:

- An *Average Power* dissipated by the device is defined as the energy dissipated per unit time and the energy needed for a given process is the integral of the power dissipated over the operation time. The instantaneous power is drawn from the power supply is proportional to the supply current and the supply voltage.
- In digital electronics, the *Propagation Delay* is the length of time which starts when the input to a logic gate becomes stable and valid, to the time that the output of that logic gate is stable and valid. Generally it is consider for the time needed for the output to achieve from 10% to 90% of its final output level when the input state changes [11]. Reducing propagation delays in digital circuits allows them to process data at a faster rate and improve overall performance.
- The *Area* of digital circuit can be measure by counting the total number of transistor used. After designing layout of circuit, the product of length and width of the circuit is considered as total area occupied by the circuit.
- Another important parameter to check the performance of digital circuit is its *Power-Delay Product* which is

considered as a figure of merit that correlate the energy efficiency of a digital logic gate. It is the product of average power consumption and the input-output delay. It has the dimension of energy, and measures the energy consumed per switching event [1].

- Other important parameter is Leakage current, Leakage current (ILeak) is exponential increases, due to reduction in VTH, L and TOX of the transistor. ILeak consist of mainly three currents like ISUB, IGATE, IBTBT. Prime objective is to reduce this leakage in idle mode of the portable electronic devices. No switching activity is performed in this mode.
- The Leakage power in digital circuits, one common problem of low swing output occurs in all logic techniques except standard Complementary metal oxide semiconductor technique. Due to low threshold voltage of transistors, drop occurs at the output voltage i.e., output does not reach to the valid high/low voltage level. The technology is continuously and rapidly evolving the production of smaller systems with minimized power dissipation; the IC industry is facing major challenges due to constraints on power density (W/cm^2) and high static (standby) and dynamic (operating) power dissipation [13-16]. The key to overcome these challenges lies in improvements in design, material and manufacturing processes.

IV. CONCLUSION:

From the literature survey, it is found that the three main sources of power dissipation in Complementary metal oxide semiconductor are: Static, Dynamic and Short Circuit power dissipation [13-14]. Static power dissipation occurs when the transistors are at steady state, either in ON state or in OFF state, whereas dynamic and short circuit power dissipation occurs during switching from one state to other state. Hence dynamic and short circuit power dissipation are jointly called switching power dissipation.The reasons for static or leakage power dissipation are leakage currents, reverse biased currents and substrate injection currents, which flow through the transistors in its steady states. Switching power dissipation arises due to the charging and discharging of output load capacitance during switching.As discussed earlier in this paper that the Sleepy keeper approach has an advantage of having less delay but it needs additional control circuit is needed. Although stack approach is easy to implement and having less leakage but more delay. Therefore, in order to minimize the delay and leakage simultaneously, hybrids approach of basic gate designing which takes the advantage of both Sleepy keeper and Sleepy Stack. This new hybrid leakage reduction technique combines sleepy technique with sleepy stack transistor.

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